PLURALITY

Leading the Multicore Revolution

Has an Israeli Start-up Succeeded Where the Giants Failed?

Plurality Ltd., a start-up company located in Netanya, Israel, presents a multicore chip with a programming model that solves the multicore dilemma

By Smadar Faigen May 2008 Technologies Magazine Vol 324

While the large, major companies in the world are still depressed looking for a multicore solution, Plurality Ltd., a start-up company in Netanya, Israel solved the multicore processor quandary using a very simple and intuitive programming model.
Founded in 2004, the company's solution combines between the hardware – 256 core-processor and software – a programming model that utilizes the entire system resources efficiently. The combination of the hardware and software is the solution to the paradox of 'the more cores on the chip, the slower the system works'.
Igor Pe'er, the CEO and Chairman stated the following:
"Our many years of experience have brought about this successful small, young company to find a solution to this large problem. The company has succeeded in producing an elegant solution to the HyperCore: Not only for a multifunctional, scalable MIMD multicore with low power dissipation and at an affordable price of only tens of dollars, it also has a very close to serial programming model that any programmer can apply."
How does the company allow the programmer to program the multicore system while not exposing the system's complexity? Pe'er emphasizes that this was accomplished after many years of research that culminated in 2004 with the founding of the company.
Dr. Nimrod Beer was the founder and today is the company's CTO as the result of his fifteen years of research on the problem of how to make mulitcores user-friendly. He began his research as a student at the Technion in Haifa under the auspices of his professor Ran Ginosar from the electrical engineering department, also one of Plurality's founders, and who serves as Director.
Igor Pe'er said, "The founding of the company completes a circle by turning theory into a real solution for the future."
The multicore dilemma today has researchers worldwide searching for solutions. Increasing the number of cores does not result in the desired Speedup. In fact it often
contributes to slowing down the processor: 32 cores will work slower than 16, 64 cores will work slower than 32 and so forth.
Intel's researcher at the recent Multicore Exhibition in the United States came to the conclusion that in order to solve this problem a hardware synchronizer, cache memory improvements and software improvements should be implemented on the system.

THE ALMOST IDEAL LINEAR SPEEDUP
Plurality L.T.D. presents new architecture based on three components:

- HW Synchonizer/Scheduler
  According to Peer it is revolutionary. Patented in the US, it was built by Dr. Nimrod Bayer, originally from Super Computers. A very similar design of this subsystem allows minimal overhead and supports very fine granulate, suitable for multicore and many cores on a chip. Pe'er emphasizes that the company is improving the current patent and also is working simultaneously on four new patents, where each one of these patents is an important component in the whole system. The synchronizer/scheduler is a hardware component which runs the cores with maximum load balance and is an effective interface between the system (the cores) and the applications. In this way the operation system overhead will be spared, while in other multicores where the operation system runs the cores, this overhead exists.
- Shared Memory
  Plurality's design connects all the cores to the same shared memory (layer 1). This fact spares the major bottle neck that is found in other multicore designs which use private cache memory for each core.
- The programming model is very easy and close to serial

> The model is based on a task map which defines the dependency between the tasks. All that the programmer needs to do is a simple division of the algorithm into specific tasks and to build the map accordingly. This dynamic implementation will run flexibly on the hardware and with maximum efficiency. Pe'er states, "This architecture allows an almost ideal linear speedup, meaning that when a number of cores arise in the processor, better performance is reached."

Peleg Aviely, one of the company's founders, is VP of engineering. He explains the real need for a new working model and differentiates from Multicore and Manycore.
Multicore includes single numerous cores in the architecture. This is the old method still in use and, as a result, in most cases you can run more than one task which is a part of different applications. Manycores respond to tens or hundreds of cores and herein lies the problem, the programmer must parallelize the same application to take advantage of the manycores.
"The main problem in parallelism," explains Aviely "is to present parallelism to the system, meaning allowing the system to deal effectively with parallelism in order to maximize the speedup."
Since we cannot expect the system to identify wide range parallelism, we need a programming model which describes the parallelism and which the architecture can utilize. The optimal situation is to ask the minimum from the programmer and to reach maximum performance.
"The difference between other companies and ours is that we developed an elegant solution including manycores with development tools which allows easy and simple programming of applications having potential to be parallelized. While with other companies, double work is needed." adds the CEO, Pe'er.
Plurality's solution is that it is suitable to the programmer whatever the number of cores, without rewriting the program. This is unique in that, until this moment, it has not been possible for existing multicore architecture. In addition, the program allows implementation not only by the multicore programmer, but also standard programmers, without any changes. From this point the system's scalability allows for the ability to add additional cores simply. "Adding cores does not change the main architecture of the processor," explains Pe'er.
Plurality's elegant solution, which combines hardware and software, also includes co-processing units which can run additional operations (e.g.: floating point operations). This fact spares the cores from doing this job, thus increasing the processor's efficiency.

DOUBLE BUSINESS PLAN
Plurality is currently registering additional patents and within a year expects to complete and produce their HyperCore with 256 cores, 90 nanometers technology in one cm with 100 Giga instructions/sec; in other words ten times faster than a Pentium with minimal power dissipation (around four watts) at a price of tens of dollars only, and not hundreds as is the cost today.
Igor Pe'er explains his business model. The company has two main business goals; one is with fabless companies to produce a chip and sell it to customers. Though the technology is suitable for general purposes, but the electronics industry like Femtocell, etc, the video market with HDV, will be able to use this co-processor.
The company already cooperates with BVR for military simulators.
In addition, Plurality collaborates with the military field. The company works with US customers' wireless infrastructure for software defined radio.

The other direction is focused on the Special Design IP Model and is targeted for the IP business, in which the company will be able to integrate the processor into the design. There is also the option for partial design as a part of the customer's architectural solution. Plurality is able to provide a partial system component as an architectural solution for customers' systems, such as shared memory subsystems or hardware synchronizer schedule. Plurality will deliver the block to the manufacturer in different configurations (64, 128, 256, or more). In this way, Plurality can address the well known companies in the IP business, and for this business development direction, it will be possible for the company to enjoy revenues from licensing new architecture suitable for the customer's requirements. In Pe'er's words, "the two directions compliment one another and this business plan will secure the company's future."

Plurality Ltd. Joined the Internationally Known MultiCore Association

Recently the International MultiCore Association (www.muticore-assocation.org), a global nonprofit organization focused on developing standards that help speed time to market for products that involve multicore implementations, announced that Plurality Ltd. is the newest member of its executive board.

"With its unique 'many-core' processor containing 256 cores, Plurality makes a notable addition to our membership," said Markus Levy, Multicore Association president. "Plurality's experience in this industry will help provide this consortium with a valuable perspective on the wide range of multicore implementations that are being deployed in the industry."

"Plurality's 256-core Hypercore processor chip, which achieves breakthrough performance per price and per watt while supporting a simple programming model, is uniquely positioned to serve as a 'general purpose accelerator,'" said Igor Pe'er, acting CEO of Plurality. "We are pleased to add this achievement to the pool of solutions offered by the members of the Multicore Association and to contribute to the common goal of creating standardized multicore solutions."

The Multicore Association is structured to provide three levels of membership, with executive board, working group, and university members. The executive board helps determine the overall direction of the organization. Working group members are eligible to participate in any of the working groups. University members may participate in any of the Multicore Association's ongoing development work, for which current projects include multicore virtual machine standardization, multicore resource management, and debug functionality to support the recently released Multicore Communication API (MCAPI).

The organization's members include ARC International, Codeplay, Enea, eSOL, Freescale Semiconductors, Imperas, Intel, Mentor Graphics, MIPS Technologies, national Instruments, NEC Electronics America, Nokia Siemens Networks, PolyCore Software, QNX, Texas Instruments, Tilera, The University of York, Wind River, and Plurality.

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